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**AMENDMENTS TO THE SPECIFICATION**

page line 26

KC  
12/18/15

Please replace paragraph [0039] with the following rewritten paragraph:

[0039] The example of a PLL 10 shown in FIG. 5, again comprises two feedback paths 131, 132. A first feedback loop 131 comprises a frequency divider 6 with a transfer function of  $1/N$ . The frequency divider 6 may for example be a conventional frequency divider. A second feedback loop 132 comprises a combined phase detector and zero device 73 with a transfer function  $K_{D_{TS}}/N, K_D$  representing a phase detector transfer function. The output 32 of the phase detector and the output 732 of the zero device 73 are connected to the inputs 201 and 202 of a second combiner device 210. ~~An output of the second combine~~ An output 203 of the second combiner device 200 is connected to the input 41 of the filter section 4. Preferably, the time-constant of the zero device 73 is set to be substantially equal to  $K_{D_{TS}}/N$ , however this is not essential.